The University of Jordan
School of Engineering
Electrical Engineering Department
2nd Semester – A.Y. 2020/2021

Course: **Digital Electronics – 0933462 (3 Cr. – Elective Course)**

Instructor: Dr. Hani Jamleh
Office: E301, Telephone: 06/5355000 ext 22848, Email: jamleh@ju.edu.jo
Office Hours: Will be posted soon

Course website: http://elearning.ju.edu.jo/

Catalog description: Building blocks and design methodologies for constructing synchronous digital systems. Bipolar TTL vs. MOS implementation technologies. Standard logic (SSI, MSI, LSI, VLSI). Programmable logic (PLD, PGA). Finite state machine design. Digital computer building blocks. Semiconductor ROM and RAM. Timing circuits. Monostable and stable multivibrators. Analog-to-digital (A/D) and digital-to-analog (D/A) converters. Using computer-aided design software (PSpice, Verilog HDL, Xilinx, etc).

Prerequisites by course: **EE** **0903361** Electronics (II) (pre-requisite)

Prerequisites by topic: Students are assumed to have a background in the following topics:
- Electrical circuit analysis techniques.
- Electronics and semiconductor fundamentals.
- Digital logic, boolean algebra, and basic knowledge of computer hardware.

Textbook: **Digital Integrated Circuits by Thomas A. DeMassa, John Wiley & Sons, 1st edition, 1995.**

References:

1. CMOS Digital Integrated Circuits Analysis & Design by Sung-Mo (S.) Kang, Yusuf Leblebici and Chul W. Kim, 4th edition, McGraw-Hill Education, 2014.
2. Digital Integrated Circuits by Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Pearson, 2nd Edition, 2003.
3. CMOS VLSI Design: A Circuits and Systems Perspective by Neil Weste and David Harris, 4th edition, Pearson, 2010.
4. CMOS Circuit Design, Layout, and Simulation by R. Jacob Baker, 3rd edition, Wiley-IEEE Press, 2010.
5. Digital Electronics: Principles and Integrated Circuits by Anil K. Maini, Wiley, 1st Edition, 2007.

6. Digital Electronics: A Practical Approach with VHDL by William Kleitz, Pearson, 9th Edition, 2011.
7. Digital Integrated Circuit Design Using Verilog and Systemverilog by Ronald W. Mehler, Newnes, 1st edition, 2014.
8. Microelectronic Circuits by Adel S. Sedra and Kenneth C. Smith, Oxford University Press, 7th edition, 2015.

Schedule: 16 Weeks, 42 lectures (50 minutes each) plus exams.

Course goals: The overall objective is to introduce the student to the design and development principles of digital electronic circuits, whether in TTL or CMOS logic.

Course learning outcomes (CLO) and relation to ABET student outcomes (SO):

Upon successful completion of this course, a student will:	[SO]
1. Be able to describe the main concepts and components of MOSFET and Bipolar Digital circuits.	[1]
2. Be able to describe the regenerative logic circuits: bistable, monostable and astable multivibartors.	[1]
3. Be able to calculate the required parameters to design and analyze various digital electronic circuits.	[1, 2]
4. Be able to analyze the different performance measures and power consumption of digital elctonic circuits.	[1]
5. Be able to design a digital electronics circuit using computer-aided design software.	[1, 2]

Course topics:	Hrs
1. Properties, definitions and performance characteristics of digital integrated circuits. Introduction to diodes and bipolar junction transistors.	3
2. Bipolar digital integrated circuits, Resistor-Transistor Logic (RTL), other logic gates, RTL fan-out, power dissipations, fan-out, etc. Basic Diode-Transistor Logic (DTL) inverter, modified DTL, DTL NAND, fanout, power dissipation, etc.	5
3. Basic Transistor-Transistor Logic (TTL) inverter, TTL NAND, multiple emitter BJT, standard TTL NAND gate, voltage transfer characteristic (VTC), power dissipation, fan-out, other TTL gates, transient analysis.	5
4. Schottky-clamped TTL (STTL), Low-Power STTL (LSTTL), Advance STTL (ASTTL), VTC, fan-out, power dissipation, transient analysis. Emitter-Coupled Logic (ECL), NOR/OR gate using ECL technology, MECL NOR/OR gate, VTC, power dissipation, fan-out, transient analysis.	6
5. Metal Oxide Semiconductor Field Effect Transistor (MOSFET), N-Channel MOS (NMOS), PMOS, modes of operation, threshold voltage, capacitances.	4
6. MOS digital circuits, NMOS inverter, resistor-loaded NMOS inverter, saturated enhancement-only loaded NMOS inverter, fan-out, power dissipation, etc.	4
7. CMOS technology, operation of CMOS inverter, fan-out, power dissipation, VTC, capacitances, RAM, ROM, etc.	4
8. Regenerative logic circuits: bistable, monostable and astable multivibrators.	3

9.	Data converters: Analog-to-Digital (A/D), Digital-to-Analog (D/A).	**3**
10.	Using computer-aided design software: PSpice, Verilog HDL, Xilinx. Project.	**3**
11.	A brief introduction to VLSI design flow and fabrication process of CMOS.	**2**

Ground rules: Attendance is required and highly encouraged. To that end, attendance will be taken every lecture. Eating and drinking are not allowed during class, and cell phones must be set to silent mode. All exams (including the final exam) should be considered cumulative. Exams are closed book. No scratch paper is allowed. You will be held responsible for all reading material assigned, even if it is not explicitly covered in lecture notes.

Assessment & grading policy:

Assignments	0%	Quizzes	0%
First Exam	30%	Projects	0%
Midterm Exam	30%	Lab Reports	0%
Final Exam	40%	Presentation	0%
		Total	**100%**

Last Revised: March 2021